AN MIC PUSH-PULL FET AMPLIFIER

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Abstract

A push-pull power amplifier, in which the required anti-phase RF voltages result from the use of inherently symmetric and frequency-independent slot line tees, is described. Measurements of the fundamental and harmonic response of this amplifier, which uses an unpackaged, two-cell FET chip and exhibits the well known fourfold impedance advantage over parallel operation, are reported.

Introduction

Push-pull operation of three terminal power devices is a well known circuit technique for minimizing distortion and/or permitting higher power operation for a set amount of distortion. In the case of microwave solid state devices (bipolar transistors or FET's) which have low input and output impedances, it offers the additional advantage of having the pair of devices connected in series rather than in parallel (push-push). Despite these and other advantages to be described, push-pull operation has not been exploited with microwave transistor amplifiers. A major reason for this has been the lack of suitable means for injecting the input signal and combining the amplified outputs of the pair of transistors in anti-phase. Attempts have been made [1,2] to build push-pull FET amplifiers at S and C bands. Dissapointing results were attributed to difficulties in developing a satisfactory balun to provide the required anti-phase input and output connections.

Slotline Tee Junction

An MIC hybrid junction, similar in operation to the well known waveguide "magic tee," has been developed for the purpose of implementation in a push-pull FET amplifier circuit.

The junction consists of a dielectric substrate with opposite planar faces metallized in prescribed patterns as shown in Figure 1. One face (the top face shown in Figure 1) is completely metallized except for a tee shaped slot as shown. The opposite face contains only a single microstrip line as shown outlined by the dashed lines representing the pattern on the bottom face of Figure 1.

The microstrip line excited at port 3 provides symmetric, in phase excitation of ports 2 and 4. The slot line excited at port 1 provides antisymmetric and hence, out-of-phase excitation of ports 2 and 4. Like the waveguide magic tee, this hybrid junction relies on bilateral symmetry to achieve its power dividing and isolation properties.

Figure 2 is an expanded view of the junction. The electric fields, due to a wave entering port 1, are shown as solid arrows and those due to a wave entering port 3 are shown as dashed arrows.

Figure 3 illustrates an equivalent circuit for a push-pull amplifier circuit.

Besides the increased input impedance of the push-pull configuration, the other major benefit which is gained in the MIC structure is the possibility of substantially reduced common lead inductance. This is possible because, as in this particular case, the two (or any even number) FET cells can be on the same chip. Since the inter-cell distance is typically extremely short, a correspondingly low source inductance is achieved. The benefits gained thereby include increased stability and a reduced gain roll-off with increasing frequency.

The short microstrip sections on the underside of the substrate are isolated from the signal frequency (f_1) propagating into the input slot line tee and out of the output slot line tee. Any even harmonics, primarily second harmonic ($f_2 = 2f_1$), which are generated by each member of the push-pull FET pair, will be in phase with each other and hence couple to the microstrip sections and be isolated from the input and output slot lines. By proper choice of the dimensions and location of these microstrip sections (retaining bilateral symmetry), a reactive termination of any arbitrary phase, $(Z_2)_{in}$ and $(Z_2)_{out}$ of figure 3, can be presented to the second harmonic while not affecting the fundamental frequency source or load impedance.

The basic symmetry of the structure also results in the reduction of spurious outputs since not only even harmonics but also even order intermodulation products and some of the possible parametric oscillations are constrained to flow in the even symmetry microstrip lines rather than the output slot lines.

Description of Test Amplifier

The push-pull characteristics of the structure were evaluated using the circuit illustrated in figure 4. In this implementation the fourth (microstrip) port of the hybrid junction was not included.

The circuit was fabricated on a 2.0" x 1.0" alumina substrate, one side of which had the input and output microstrip lines, and the other side the slot line circuitry. The overall 2.0" x 1.0" dimensions were chosen solely as a matter of convenience and flexibility. A pair of FET cells (on one chip) and several capacitors are on the slot side of the substrate. The capacitors (four) terminate short lengths of slot line which are used to shunt-resonate both the input and output. The FET's used here were not state-of-the-art devices, but adequate for the evaluation of the circuit. Figure 5 illustrates the chip geometry. Two of the three cells were used and only 3 of the 4 drains were connected in each cell. Figure 6 illustrates the calculated impedance locii for a single cell, a push-pull pair, and (for purposes of comparison) a push-push (parallel) pair. Figure 7 illustrates the single cell equivalent circuit. The chip (.040" x .050")is mounted such that the two cells in use are equidistant from the center line of the input/output slots. The gate and drain wires are mounted across their respective slots also in such a way as to preserve physical symmetry.

All slot line impedances were chosen to be a nominal 50 ohms. Input and output lines were on microstrip and the transition to slot line was made via the crossed $\lambda/4$ stubs shown in figure 4. The center frequency was chosen to be 6.0 GHz.

Experimental Results

Figure 8 gives the P_{out} and P_{in} characteristic of the amplifier at 6.0 GHz. All data is referred to the chip terminals and assumes 0.6 dB loss in both the input and output circuits. Small signal gain is 11.5 dB and at the point of maximum power-added the gain is 6.5 dB and the output power is 780 mW. The maximum power added is 600 mW.

One of the questions which arose when RF testing began was whether the amplifier was actually operating in a push-pull mode. The measurement technique which was decided on made use of the property of the push-pull mode which predicts that even harmonics of the input will not be present in the output if the transistors are perfectly matched. If the devices are not identical, even harmonics will be present, but in an intensity lower than in a non-push-pull configuration.

Since the amplifier was designed to operate at 6 GHz, the second harmonic would occur at 12 GHz. At 12 GHz however, the slot line and microstrip input and output are decoupled since the $\lambda/4$ sections are now $\lambda/2$ long. This problem was overcome, however, by injecting a signal at 3 GHz. The second harmonic is now at 6 GHz and will couple to the microstrip. The reduction of the input frequency should not affect the push-pull nature of the circuit since the slot-line tee's symmetry properties are independent of frequency.

The devices were biased close to a class B condition so that with a moderate input signal harmonics would be generated. The input RF power was +17 dBm, at 3.0 GHz. The output power was measured at 3.0, 6.0, 9.0, 12.0 and 15.0 GHz using a spectrum analyzer. The outputs were measured under two conditions, that is both cells biased (push-pull) and only one cell biased (single ended). Table 1 presents the resultant data as a ratio of harmonic power to fundamental power for the two conditions above. The subscripts refer to harmonic number.

Table 1

	P2/P1	P3/P1	P4/P1	P5/P1
Push-Pull	-26 dB	-31	-47	-40
Single Ended	-12 dB	-30	-40	-41

Note that for the even harmonics, that is 6.0 GHz and 12.0 GHz, substantial drops in these ratios were encountered in going from the single ended case to the push-pull case. For the odd harmonics, 9.0 and 15.0 GHz, the ratios did not change appreciably. These results appear to substantiate the push-pull nature of the circuit.

Conclusions

The slot line tee junction has been shown to be adaptable to a push-pull mode of operation for FET's and bipolar transistors. The benefits of this type of amplifier structure are:

1) A fourfold increase in impedance level over a parallel connection, for the same output power.

2) A minimum common lead inductance if two adjacent cells on the same chip are used resulting in a slower gain vs frequency roll-off and under most conditions, improved stability.

3) A theoretically expanded linear range as well as reduced intermodulation distortion and higher output power if second harmonic tuning is used.

Acknowledgements

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References

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2. L. S. Napoli and J. J. Hughes, "High Power C-Band Microwave Integrated Transistor Amplifiers, Second Semi-annual report ECOM-0223-2, October, 1973. Reports Control System OSD-1366, DA Project No. 15662705A440 Task 02.

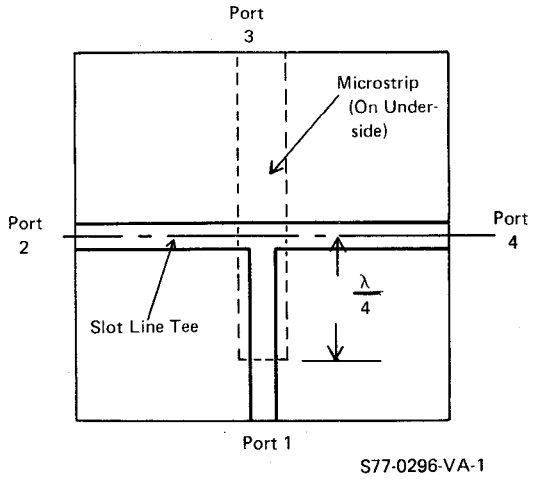

FIGURE 1 - Configuration of slot/microstrip hybrid junction.

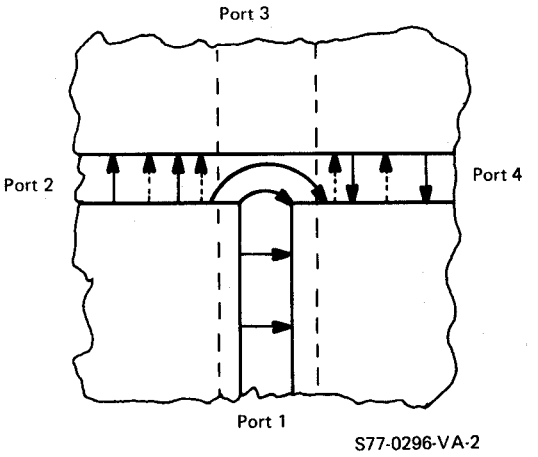

FIGURE 2 - Expanded view of slot/microstrip hybrid junction showing electric field orientation for inputs at Port 1 (solid arrows) and Port 3 (dashed arrows).

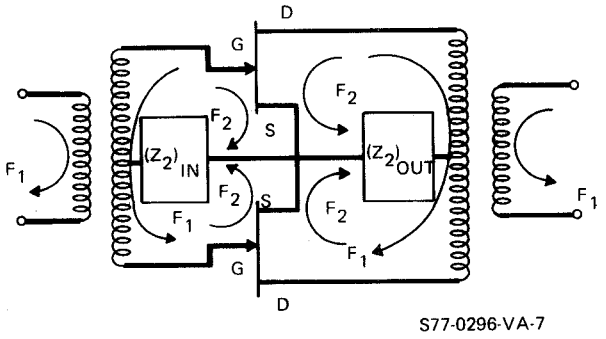

FIGURE 3 - Push-pull FET equivalent circuit. For a perfectly matched pair, even harmonics of the input frequency are represented by F_2.

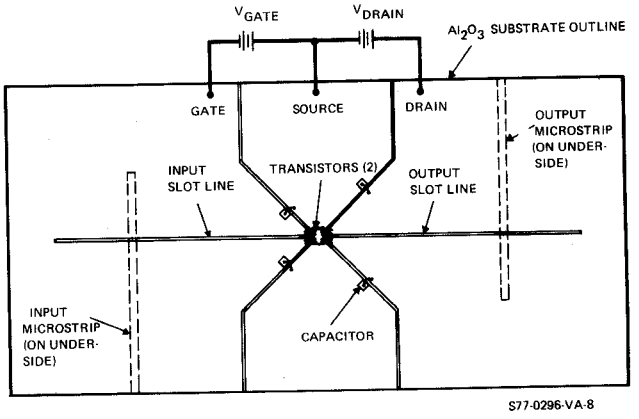

FIGURE 4 - Implementation of push-pull circuit on 2.0" x 1.0" substrate. The FET chip is mounted on the substrate.

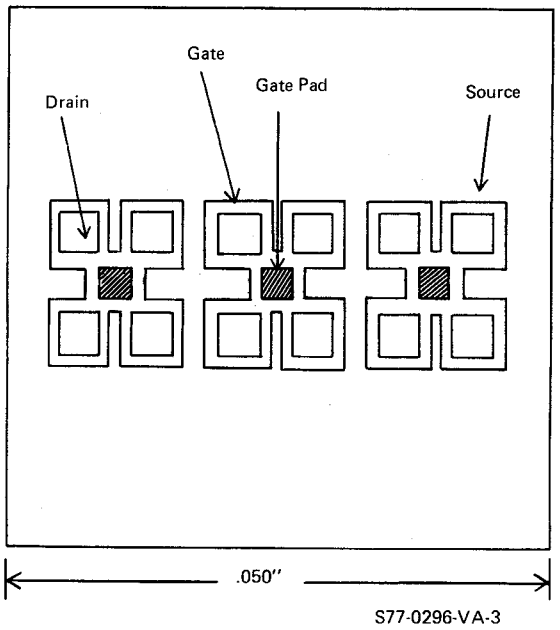

FIGURE 5 - Outline of FET chip.

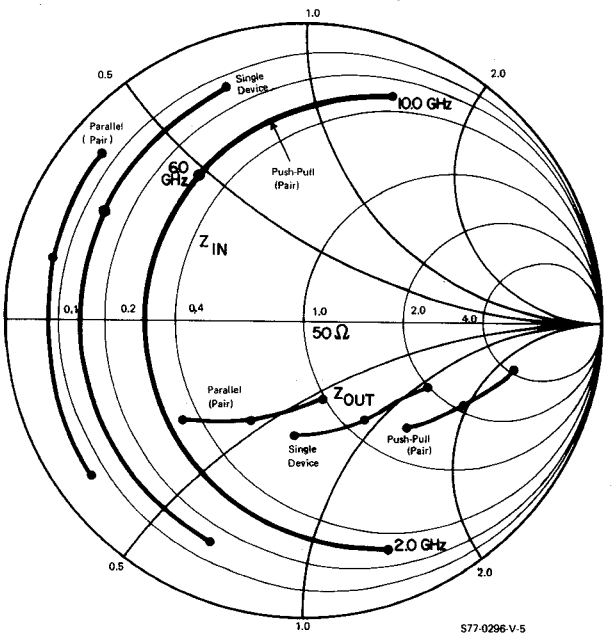

FIGURE 6 - Impedance loci for push-pull pair, single device and parallel pair. Single device equivalent circuit is given in Figure 7.

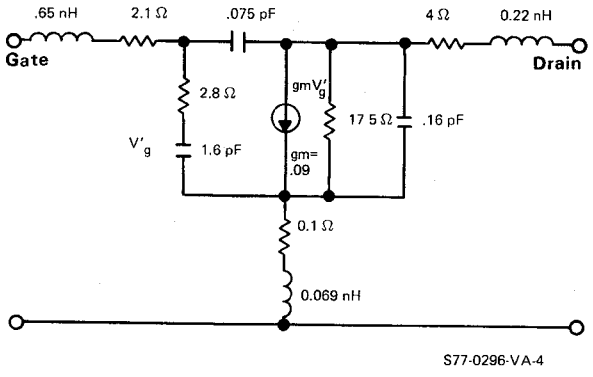

FIGURE 7 - Equivalent circuit of Westinghouse 1400 μ device with 3 out of 4 drain pads used.

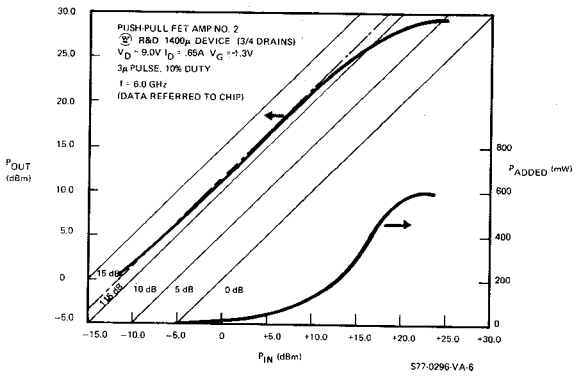

FIGURE 8 - Output power and added power versus input power for push-pull amplifier at 6.0 GHz.